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DATE: Monday, August 02, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L20	L19 and (carrier near3 (recover$3 or track$3))	22
☐	L19	L18 and l17	409
☐	L18	(375/$3.ccls. or 370/$3.ccls.)	91801
☐	L17	((plural$3 or multipl$3) near4 (frame$3 near3 sync$9))	975
☐	L16	hierarchal and ((plural$3 or multipl$3) near4 (frame$3 near3 sync$9))	0
☐	L15	hierarchal same ((plural$3 or multipl$3) near4 (frame$3 near3 sync$9))	0
☐	L14	L13 and (frame near3 sync$9)	42
☐	L13	375/326.ccls.	450
☐	L12	L11 and 375/326.ccls.	0
☐	L11	((plural$3 or multi$34) near2 (frequenc$3 near3 range$2)) and (frame near3 sync$9)	18
☐	L10	((plural$3 or multi$34) near2 (frequenc$3 near3 error$2)) and (frame near3 sync$9)	6
☐	L9	L8 and (de adj map$4)	0
☐	L8	l6 and l5	25
☐	L7	370/509.ccls. or 370/503.ccls. or 370/510.ccls. or 370/511.ccls. or 370/512.ccls. or 370/513.ccls. or 370/514.ccls. or 375/362.ccls. or 375/363.ccls. or 375/364.ccls. or 375/365.ccls. or 375/366.ccls. or 375/367.ccls. or 375/368.ccls.	6485
☐	L6	375/279.ccls. or 375/280.ccls. or 375/281.ccls. or 375/261.ccls. or 375/316.ccls. or 375/330.ccls. or 375/331.ccls. or 375/340.ccls.	3341
☐	L5	(carrier near3 (track$3 or recover$3)) and (frame near3 sync$9)	511
☐	L4	((plural$3 or multi$34) near2 (frequenc$3 near3 error$2)) and (carrier near3 (track$3 or recover$3)) and (frame near3 sync$9)	0
☐	L3	((plural$3 or multi$34) near2 (frequenc$3 near3 rang$2)) and (carrier near3 (track$3 or recover$3)) and (frame near3 sync$9)	1
☐	L2	((plural$3 or multi$34) near2 (frequenc$3 near2 rang$2)) and (carrier near3 recover$3) and (frame near3 sync$9)	0
☐	L1	((plural$3 or multi$34) near2 (frequenc$3 near2 rang$2)) same (carrier near3 recover$3) same (frame near3 sync$9)	0

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L3: Entry 1 of 1 File: USPT Jun 6, 1989

DOCUMENT-IDENTIFIER: US 4837786 A
** See image for Certificate of Correction **
TITLE: Technique for mitigating rain fading in a satellite communications system using quadrature phase shift keying

Detailed Description Text (7):
Typically, the data transmission schemes used to transmit the data in either of the foregoing exemplary systems use some form of multiplexing. For example, one scheme which may be seen in the system of FIG. 1 is time division multiplexing (TDM). In time division multiplexing, the data transmitted from one ground station to the satellite and then to another ground station is included in a digital data stream that is time division multiplexed. As is well known in the art, in time division multiplexing, the digital data is transmitted in frames having a predetermined number of data information bits in each frame. Within each frame, a predetermined number of bits are used for frame synchronization and identification and the remaining bits are used to define time slots and to provide error checking capabilities. For example, FIG. 2 illustrates a highly simplified frame of data 150 that is transmitted from the transmitter 122 to each of the receivers 134, 136, 138. The exemplary frame of data 150 typically includes a synchronization pattern 152 that designates the beginning of each frame 150 and is utilized to synchronize circuitry within each of the receivers 134, 136, 138 with the transmitted data. The frame 150 may advantageously include a predetermined number of bits of data that comprise a frame count 154 that is incremented by the data source 142 once for each frame. Following the frame count 154 is a time slot 156 which comprises a predetermined number of bits of data that are directed to the receiver 134. The time slot 156 is followed by a time slot 158 which comprises a predetermined number of bits directed to the receiver 136, which is in turn followed by a time slot 160 comprising a predetermined number of bits directed to the receiver 138. The frame 150 is followed by subsequent frames, each beginning with the synchronization pattern 152. In the exemplary addressed operation, each of the receivers 134, 136, 138 receives all the information transmitted by the transmitter 122. Within each of the receivers 134, 136, 138, demultiplexing logic selectively extracts the data information bits intended for the respective receiver. For example, the receiver 138 advantageously selects only the data information bits in the time slot 156 in each frame 150 and provides the output information to the respective local network 148. One skilled in the art will understand that there are a number of different time division multiplexing techniques, each having their own particular advantages and disadvantages.

Detailed Description Text (22):
The transmitter 212 mixes the phase modulated intermediate frequency on the line 216 with a frequency in the range of 14.0-14.5 GHz and generates a signal that is transmitted via the transmitting antenna 210 towards the satellite 202. The satellite 202 is advantageously a conventional satellite that includes a number of transponders that receive signals in the 14.0-14.5 GHz frequency range from a plurality of transmitting ground stations, such as the ground station 200, and retransmit the received signals towards the ground at frequencies in the range of 11.7-12.2 GHz to be received by a plurality of receiving ground stations, such as the ground station 204. Thus, for the purpose of the present invention the

satellite 202 serves as a frequency translating relay between the transmitting ground station 200 and the receiving ground station 204.

Detailed Description Text (33):
Within the tracking circuits block 502, all essential demodulation tracking is executed and both the P channel and Q channel signals are extracted from the input samples on the X bus 504 and the Y bus 506 and are provided as output signals on the P data bus 470 and the Q data bus 472, respectively to the decoder circuit 480. The tracking circuits block 502 provides carrier phase tracking, automatic frequency control signal generation, automatic gain control signal generation, chip time tracking and clock generation, removal of the Q channel spreading sequence, generation of the P and Q data output streams on the buses 470 and 472, respectively, and the initial acquisition procedures discussed above. The X sample inputs on the X bus 504 and the Y sample inputs on the Y bus 506 from the synchronous translator and quantizer block 500 are provided at a rate that is twice the chip rate. Thus, in the preferred embodiments, wherein the P channel operates at the chip rate, the outputs of the two quantizers are provided at twice the P channel data rate. As well as providing the P data output on the P data bus 470 and the Q data output on the Q data bus 472, the tracking circuits block 502 also provides the P clock on the line 474, and the Q clock on the line 476. In addition, the tracking circuits block 502 provides the fade indicator on the line 478, as discussed above.

Detailed Description Text (45):
The despread Q channel signal and the despread P channel signal are used together in the phase/frequency tracking block 604 to derive an indication of the angular tracking error .delta. which serves as the input variable to the tracking loop during routine carrier tracking after the signal is acquired. This error variable has a markedly higher signal-to-noise ratio than is available by using the basic chip variables from the synchronous translator and quantizer block 500 without despreading. This feature, together with the narrow loop bandwidth which is established as the final step of the acquisition procedure, is a fundamental basis for the ability of the present invention to maintain synchronization of the coordinate system P.sub.RS, Q.sub.RS with the coordinate system P.sub.S, Q.sub.S in the presence of fading caused by rain attenuation or other causes.

Detailed Description Text (56):
The bandwidth reduction process causes the effective loop bandwidth of the tracking loop to be varied by degrees from the rather wide value that pertains during acquisition to a final value in the range of 100 Hz. This value of bandwidth yields an optimum trade-off in terms of minimizing the phase tracking jitter against the competing demands of thermal noise and phase noise. When the phase tracking loop is in the routine tracking mode with the bandwidth reduced to its optimum value, the phase/frequency tracking block 604 will maintain carrier phase tracking at a Q channel energy-per-dimension-to-noise ratio (E.sub.d /N.sub.o) of -1 dB or higher. This corresponds to a chip-energy-to-noise ratio (E.sub.c /N.sub.o) of -1 minus log (N) dB or -10 dB in the representative case where N equals 8. For a normal clear sky reading of +4 dB for E.sub.c /N.sub.o, the demodulator described herein can sustain a rain fade of 14 dB while retaining the integrity of the carrier tracking function.

Detailed Description Text (62):
At the point in the acquisition cycle where despreading of the Q channel is achieved, the clock oscillator and timing tracking loop within the clock oscillator and timing tracking block 606 changes its tracking strategy to exploit the improved signal to noise ratio available from the despread Q data output on the line 472. This processing yields a clock generation process which is capable of maintaining correct clock operation at all signal to noise ratios for which the phase/frequency tracking block 604 can maintain carrier tracking. This approach strongly enhances the reliability of the resultant error signal for timing tracking.

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L8: Entry 25 of 25 File: USPT Aug 18, 1981

DOCUMENT-IDENTIFIER: US 4285062 A
** See image for Certificate of Correction **
TITLE: Digital multi-level multi-phase modulation communication system

Abstract Text (1):
A digital multi-level multi-phase modulation system utilizes quaternary differential encoding and decoding of only the first two of N digital signal trains. A decision circuit is used to examine the frame pulses in one of the first two signal trains and in at least one of the remaining signal trains and generates output signals which can be used in a gate circuit to resolve the phase-lock ambiguity of the recovered carrier and thereby reproduce the original N signal trains.

Brief Summary Text (9):
This invention provides a digital multi-level multi-phase modulation communication system having a transmitting section and a receiving section: wherein the transmitting section includes first means (8) for performing quaternary differential encoding on the first two trains (S.sub.1, S.sub.2) of N trains (N is an integer of 4 or more) of digital signal, a frame pulse being included in (N-1) of said digital signal trains, to generate a first pair of digital signals (S.sub.1 ', S.sub.2 '); and second means (2-7, 10, 11) for generating a modulated wave by performing multi-level multi-phase modulation on the carrier with a first set of (N-2) digital signals comprising the first (N-2) trains of digital signal (S.sub.3 -S.sub.n) the first two trains of digital signal, and with the second two trains of digital signal; and wherein the receiving section includes third means (12-14) for performing coherent detection and multi-level decision on the modulated wave to generate a second set of (N-2) digital signals (S.sub.3 "-S.sub.N ") and a second pair of digital signals (S.sub.1 ",S.sub.2 ") corresponding to the first set of (N-2) digital signals and the first pair of digital signals, respectively, fourth means (15) for performing quaternary differential decoding on the second pair of digital signals (S.sub.1 ",S.sub.2 ") to generate the first two trains of digital signal, fifth means (17) for establishing frame synchronism by means of the output signal (S.sub.2) from the fourth means, sixth means (21-23) responsive to the output of the fifth means for extracting a frame pulse corresponding to the frame pulse included in the second set of (N-2) trains of digital signal and in the output signal of the fourth means, seventh means (24, 25) responsive to the output of the sixth means for generating a control signal (G.sub.1, G.sub.2) representing the phase-locking state of the carrier recovered in said third means, and eighth means (19) responsive to the control signal for converting the second set of (N-2) digital signals into the same trains as the first set of (N-2) digital signals.

Detailed Description Text (2):
In FIG. 1, reference numeral 101 designates a transmitting section; 102, a receiving section; 1, a transmit data processing unit; 2, a transmit local oscillator; 3, a divider; 4, a .pi./2 phase shifter; 5 and 6, each an amplitude modulator; 7, a combiner; 8 and 9, each a summing logic circuit; 10 and 11, each a D/A converter circuit; 12, a QAM demodulator circuit; 13 and 14, each an A/D converter circuit; 15 and 16, each a subtracting logic circuit; 17, a frame synchronizer circuit; and 18, a receive data processing unit. In the transmitting

section 101, input data signals DATA 1 and 2 are supplied to the transmit data processing unit 1 where the symbol rates of DATA 1 and 2 are changed for adding frame pulses for frame synchronization, stuff pulses for providing synchronism between input signals, and pulses for order-wire channel to the DATA 1 and 2 which are then deserialized to generate four signal trains S.sub.1 to S.sub.4. While the above description assumes the supply of two input DATA 1 and 2, it is to be understood that any number can be selected for the number of input signal trains.

Detailed Description Text (3):
The pair of signals S.sub.1 and S.sub.2 and that of S.sub.3 and S.sub.4 are supplied to the summing logic circuits 8 and 9, respectively, where they are subjected to quaternary differential encoding to generate a pair of signals S.sub.1 ' and S.sub.2 ' and that of S.sub.3 ' and S.sub.4 '. The signals S.sub.1 ' and S.sub.3 ' are supplied to the D/A converter circuit 10 to be converted to a 4-level signal P, and the signals S.sub.2 ' and S.sub.4 ' supplied to the D/A converter 11 to be converted to a 4-level signal Q. The signals P and Q are supplied to the amplitude modulators 5 and 6, respectively. To the other input of the modulator 5 is supplied a carrier obtained by branching in the divider 3 the carrier from the transmit local oscillator 2, and to the other input of the modulator 6 is supplied a carrier which is in quadrature with the carrier supplied to the modulator 5 and which is obtained by being passed through the .pi./2 phase shifter 4 downstream of the divider 3. These carriers are modulated with the signals Q and P, combined together in the combiner 7 to achieve 16 QAM as illustrated in FIG. 2, which is then supplied to the receiving section 102. In the receiving section 102, the QAM demodulator circuit 12 performs coherent detection to demodulate the 4-level signals P and Q which are fed to the A/D converter circuits 13 and 14 for 4-level decision to generate two pairs of 2-level digital signals S.sub.1 " and S.sub.3 " as well as S.sub.2 " and S.sub.4 ". These signal pairs correspond to the signal pairs S.sub.1 ' and S.sub.3 ' as well as S.sub.2 ' and S.sub.4 ', respectively, generated in the transmitting section 101, but due to the phase ambiguity in phase-locking with the reference carrier recovered at the QAM demodulator circuit 12, their pattern arrays may or may not agree with digital signals S.sub.1 " and S.sub.4 '. Therefore, the pair of signals S.sub.1 " and S.sub.2 " as well as the pair of signals S.sub.3 " and S.sub.4 " are subjected to quaternary differential decoding in the subtracting logic circuits 15 and 16, respectively, to provide signals S.sub.1 to S.sub.4 that agree with the signals fed S.sub.1 to S.sub.4. The signal S.sub.4 is branched and supplied to the frame synchronizer circuit 17 (for a possible embodiment of the circuit, see U.S. Pat. No. 3,978,285) for achieving frame synchronization to reproduce a frame timing pulse FS. The signal FS is supplied to the receive data processing unit 18. In the unit 18, through the conversion process which is the reverse of the process performed in the transmit data processing unit 1, the signal FS removes from the input signals S.sub.1 to S.sub.4 all additional signals that have been inserted into said signals at the transmit data processing unit 1, thus reproducing signals in agreement with the original signals DATA 1 and 2. As described above, the conventional 16 QAM communication system of FIG. 1 has the two quaternary differential coding circuits at the transmitting and receiving sections, respectively. Accordingly, a error rate in this system is about twice as high as that in the system without any differential coding circuit.

Detailed Description Text (5):
Referring now to the receiving section 202, the 4-level signals P' and Q' demodulated in the QAM demodulator 12 are supplied to the A/D converter circuits 13 and 14, respectively, which perform 4-level decision to generate a pair of signals S.sub.1 " and S.sub.3 " and that of signals S.sub.2 " and S.sub.4 ". The signals S.sub.1 " and S.sub.2 " that correspond to the signals S.sub.1 and S.sub.2 are supplied to the subtracting logic circuit 15 where they are subjected to quaternary differential decoding to reproduce signals that agree with the signals S.sub.1 and S.sub.2. The signal S.sub.2 is branched into two, one of which is supplied to the frame synchronizer circuit 17 to establish frame synchronization for reproduction

of the frame timing signal FS. The signals S.sub.3 ", S.sub.4 ", S.sub.2 and FS are supplied to a decision circuit 20 which generates decision signals G.sub.1 and G.sub.2 representing phase-locking state of the carrier recovered in the QAM demodulator circuit 12. The decision signals G.sub.1 and G.sub.2 are supplied to the gate circuit 19. The gate circuit 19 uses the decision signals G.sub.1 and G.sub.2 to control the input signals S.sub.3 " and S.sub.4 " so that they agree with the signals S.sub.3 and S.sub.4 regardless of the phase-locking state of the recovered carrier in the QAM demodulator circuit 12, and as a result the circuit 19 generates signals S.sub.3 and S.sub.4. The thus reproduced signals S.sub.1 to S.sub.4 are supplied to the receive data processing unit 18 which is responsive to the signal FS to produce signals DATA 1 and 2 by removing the additional bits inserted in the original signals in the transmit data processing unit 1.

Detailed Description Text (7):
Referring to FIG. 4, signals S.sub.2, S.sub.3 " and S.sub.4 " are supplied to the D-type flip-flops 21 to 23, respectively, where they are sampled with the frame timing pulse FS, and as a result, the frame pulse M is extracted from each signal. Table 1a below shows the change in the signals S.sub.3 " and S.sub.4 " depending on the phase-locking state of the recovered carrier at the QAM demodulator 12. Table 1b shows the condition of the frame pulse M extracted from the signals S.sub.3 " and S.sub.4 ", following the change indicated in Table 1a. The outputs of the flip-flops 21 and 23 are supplied to the Exclusive-OR gates 24 and 25 where an Exclusive-OR operation is applied to the outputs to generate decision signals G.sub.1 and G.sub.2. respectively, as identified in Table 1c below.

Current US Cross Reference Classification (3):
375/281

CLAIMS:

1. A digital multi-level multi-phase modulation communication system having a transmitting section and a receiving section, wherein said transmitting section includes:

first means for performing quarternary differential encoding on the first two trains of N digital signal trains (N is an integer of 4 or more), a frame pulse being included in at least three of said N digital signal trains, to generate a first pair of digital signals; and

second means for generating a modulated wave by performing multi-level multi-phase modulation on a carrier with a first set of digital signals comprising the remaining (n-2) trains of said N digital signal trains and said first pair of digital signals; and wherein said receiving section includes:

third means for performing coherent detection and multi-level decision on said modulated wave to recover said carrier and generate a second set of digital signals and a second pair of digital signals corresponding to said remaining (N-2) trains of said N digital signal trains and said first pair of digital signals respectively;

fourth means for performing quaternary differential decoding on said second pair of digital signals to generate said first two trains of digital signal;

fifth means for generating a frame synchronization output signal and establishing frame synchronism by means of the output signal from said fourth means;

sixth means responsive to the output of said fifth means for extracting frame pulses corresponding to said frame pulses included in said remaining (N-2) trains of said N digital signal trains and in the output signal of said fourth means;

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seventh means responsive to the output of said sixth means for generating a control signal representing the phase-locking state of the carrier recovered in said third means; and

eighth means responsive to said control signal for converting said second set of digital signals into the same trains as said remaining (N-2) trains of said N digital signal trains.

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L10: Entry 5 of 6 File: USPT Sep 14, 1999

DOCUMENT-IDENTIFIER: US 5953649 A
TITLE: Signal acquisition in a satellite telephone system

Brief Summary Text (9):
The object of the present invention is to introduce a method for signal acquisition, frame synchronisation and elimination of frequency errors in a multi-frequency communications system by utilising a transmission which is in advance arranged to a certain rhythmic pattern on a given control channel. Another object of the invention is to achieve a system which operates quickly and reliably in varying reception conditions and can adapt itself to changing conditions.

Detailed Description Text (32):
When the more refined frame synchronisation (step 24 in FIG. 2) gives the calculated location of the reference sequence in successive bursts, so that the difference is one symbol to one direction or the other, the underlying ambiguity caused by the sampling technique can be clarified by many different ways. For example, the receiver can first process side by side two different signals synchronised according to different frame synchronisation points, whereafter that frame synchronisation point which gives better results is chosen as the final point. Another alternative is to shift the above mentioned digital sampling window forward or backward for half a symbol and then to study whether this improves the signal quality. If the shift took place in a wrong direction, the frame synchronisation point is shifted to the opposite direction for the length of one whole symbol.

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DOCUMENT-IDENTIFIER: US 5953649 A
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